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FAULT SIMULATION DEVICE
[USTROYSTVO DLYA IMITATSII NEISPRAVNOSTEI]

S. L. ULYBIN

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INVENTOR	(72): S. L. ULYBIN
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71: The Ulyanovsk Research and Industrial Complex - The Center for Microelectronics and Automation Application in Machine Building

72: S. L. Ulybin

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54: FAULT SIMULATION DEVICE

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57: The present invention is used for simulating faults in the calculation process. The objective of the invention is to expand functional capabilities as a result

of forming a cascade of several devices to ensure defining the place for fault insertion under any number of conditions. The number of conditions that defines the place for fault insertion is limited only by the number of devices within the cascade. The initial signal enters at input points 9, 10, and 19, along with the record indicator and reset signal, thus preparing the device for operation. At that time, counter 1 records address where the fault needs to be inserted. Input points 11 and 12 of the computer receive current addresses and address identifiers. If the contents of counter 1 match with the input address, comparison block 3, trigger 4 and driver 5 produce a fault-simulating signal at the output point 13. Counter 2, elements OR 6, 7, element AND 8 and time markers input at entry point 18 are used for automated modification of the fault-insertion place. Input points 14 and 15 and output points 16 and 17 are used for connecting several devices into cascade. 2 figures

The present invention refers to electronics and computers and may be used for testing the fault tolerance of computer systems.

The objective of the invention is to expand functional capabilities as a result of forming a cascade of several

devices to ensure defining the place for fault insertion under any number of conditions.

Fig. 1 shows a model of a device for fault simulation; and Fig. 2 shows a model of connection fault simulation devices into a cascade.

The device contains two counters - 1 and 2, comparison block 3, driver 4, impulse former 5, two OR elements 6 and 7, AND element 8, input 9 for initial address definition, input 10 for record, input 11 of the current address, input 12 for the address identifier, output 13 for fault simulation, first 14 and second 15 entry points for cascading, first 16 and second 17 exit points for cascading, input 18 for time markers, and reset input 19.

The connection model (Figure 2) demonstrates a cascade from n of fault-simulation devices 20. The devices allow for modifying the place for fault insertion, both manually (using software) and automatically (using hardware).

When connecting one device to the computing system (Figure 1) to the first input 1 of cascading, the level of logic component 0 is specified. If it is needed to modify the place for fault insertion, then output 13 should be connected with input 15 of the device, while time markers are to be transmitted to input 18. The frequency of time markers is selected so that it ensures overflow of counter 2 after the period of time specified for fault simulation at one address. At the same time, the second output 17 of the cascading of the device is the output of the identifier signaling the end of testing fault resistance of the computer system.

When n of devices is connected to the cascade (Figure 2), the first output 16 of the cascading i device 20 (i= 1, … n-1) is connected with the first entry point of cascading 14 of the (i+1) device 20. The output 13 of n device 20 is the output point for the cascade fault simulation. Furthermore, it is connected with the input 14 of the first device 20. If it is needed to ensure automatic modification of the fault insertion, an additional connection is

required. Output 13 of the n device 20 needs to be connected with the second output 15 of cascading n device 20. The second output of cascading 17 of (i+1) device 20 needs to be connected with the second input 15 of cascading i device 20. Inputs 18 of the device should have time markers transmitted frequency, which should be specified so that counter 2 is overflowing following the period of time specified by the developer of the computing system. At the same time, output 17 of the first device 20 is the exit point for the identifier of completed test of fault-resistance of the computing system.

Inputs 11 of device 20 are connected with the outputs of the computing system addresses that specify the point in the calculation process at which the fault is inserted. Depending on the specific implementation of the computing system inputs 11 of device 20 may be connected, for example, (with n=3): for the first device 20 - with the output of the page register (with the page organization of the computing system memory); for the second device - with the output of the command counter; for the third device 20 - with the output point of the micro command counter where micro command addresses are being formed.

Inputs 12 of device 20 are then connected with: for the first device 20 - with the page register record point;

for the second device 20 - with the output for the memory address identifier from the command counter; for the third device 20 - with the output of the micro command memory address identifier from the counter.

Inputs 18 of device 20 are connected with the output of time markers, the frequency of which ensures overflow of counters 2 after the time adequate for the following showing at inputs 11: for the first device 20 - of the number of memory page specified by counter 1; for the second device 20 - of the command address specified by counter 1; for the third device 20 - of the micro command address specified by counter 1.

The device is prepared for operation in the following manner:

Information is transmitted (for instance, from the switch distribution panel) to the input 9 of the device, which will be its initial address for fault simulation. This information from input 9 is then transmitted to the information input of counter 1. The signal (for instance, from the problem board key) is transmitted to input 10, which is then transmitted to the record entry point of counter 1 and records the code of the initial address in the counter. Then, a signal (for instance, from the problem board key) is transmitted to input 19, which is sent to the

first entry of the OR element 7. At the exit point of the OR element 7 the signal appears, which is then transmitted to the input of the counter reset 2 and resets its value back to zero. After this is completed, the device is ready to operate.

The device operates as follows:

When the calculating system is in use, the codes of the system pages are transmitted to input 11 of the first device.

From that input 11, these codes are then transmitted to the first comparison block 3, while the code from the counter output 1 is transferred to its second input. The signal from the output of comparison block 3 is then transferred to the trigger information input 4.

Signals from the page register of the computing system are transmitted to input 12 of the first device. From input 12, these signals are transferred to the record input of trigger 4. The reset input of trigger 4, which is connected with the inverse entry point of the AND element 8 and with input 14 of the device, the low potential is transmitted from output 13 of the third device (Figure 2), which does not interfere with the functioning of trigger 4. When runs at the inputs of comparison block 3 do not match, its output shows the value "0," which is then recorded to trigger 4 by the signal from input 12. At the same time, the singular potential from inverse output of trigger 4 is transmitted to input 16 of the device. From input 16 of the first device the singular potential is then transmitted to input 14 of the second device. Unit impulse from input 14 supports the zero status of trigger 4 and blocks AND element 8 of the second device. Unit impulse from the inverse output of trigger 4 of the second device supports

the zero status of trigger 4 and blocks element AND 8 of the third device.

Time markers are transmitted to inputs 18 of the device. From input 18, time markers are transmitted to the second input of AND element 8 of devices. Since AND elements 8 of the second and third devices are blocked, the time markers will appear only at the output of the AND element 8 of the first device. Then they are transmitted to the counter 2 entry points. If during the period of time equal to $T_1 = 21\ t_1$ (where 1 is the counter 2 capacity, and t_1 is the period of time marker sequence when transmitted to input 18 of the first device) the computing system did not address the page of memory whose code matches the code on counter 1, then counter 2 will overflow. The output of counter 1 will show a signal that thought the OR element 6 is then transmitted to the calculation input of counter 1. The contents of counter 1 will then increase by one. Therefore, with the extended non-occurrence of the tracked condition in the computing system (in this example, the given code of the memory page), the condition will modify automatically.

If codes arriving at inputs of comparison block 3 match, its output will show "1," which will then be a recorder to trigger 4 by a signal from input 12. Singular

potential from the direct output of trigger 4 will then be transmitted to input of driver 5, as well as to the second input of the OR element 7. Driver 5 forms a signal at its output. At the output of the OR element 7, a singular potential will appear, which is then transmitted to the reset input of counter 2, resetting it to zero, and supports its zero statute. Zero potential from the inverse output of trigger 4 is transmitted to output 16 of the first device. Then zero potential is transferred to the reset input of trigger 4 of the second device, allowing its functioning, and to the inverse input of AND element 8 of the second device, allowing transfer of time markers from input 18 through it. If during the period of time equal to $T_2 = 21\ t_2$ (where t_2 is the period of time marker sequence when transmitted to input 18 of the second device) the computing system does not address the command whose address matches the code on counter 1, then counter 2 will overflow. The contents of counter 1 will then increase by one.

When code maintained at counter 1 of the second device and the address of the command transmitted from the computing system to input 11 of the second device match, trigger 4 will be set at the singular position. Thus, the

function of counter 2 of the second device is blocked and function of trigger 4 of the third device is allowed. Furthermore, time markers from input 18 begin being transmitted to counter 2 of the third device. If during the period of time equal to $T_3 = 21\ t_3$ (where t_3 is the period of time marker sequence when transmitted to input 18 of the second device) the computing system does not address the micro command whose address matches the code on counter 1 of the third device, then counter 2 will overflow. The contents of counter 1 will then increase by one.

When the code stored on counter 1 of the third device with the micro command address transmitted from the computing system to input 11 of the third device, trigger 4 is set to the singular position. At the same time a fault simulating signal is formed at the driver output 5, which is then transmitted to the output 13 of the device. From output 13 of the third device this signal is then transmitted to input 15 of the third device and to input 14 of the first device. From input 15 of the third device the signal is transmitted through the OR element 6 to the complementary input of counter 1, thus increasing its contents by "1." Therefore, the automated modification of fault-simulating addresses is guaranteed.

From input 14 of the first device, the signal resets trigger 4, which releases counter 2 of the first device as well as resets triggers 4 and blocks time markers in the second and third devices.

The next fault simulation will be completed when the program enters the memory page whose code is listed in counter 1 of the first device, as well as with the completion of micro command whose address is formed again at counter 1 of the third device and the command whose address matches the code on counter 1 of the second device.

After the fault is set in all micro commands following this command, counter 1 of the third device will overflow. The overflow signal from the output of counter 1 is transmitted to input 15 of the second device, from input 15 the signal is transmitted to the complementary input of counter 1 of the second device using OR element 6, thus increasing contents of counter 1 by "1."

After the fault is set in all micro commands of all commands available on the specified memory page, counter 1 of the second device will overflow. The overflow signal from the output of counter 1 is transmitted to input 15 of the first device, using output 17 of the second device. From input 15 this signal is transmitted to the complementary input of counter 1 of the first device using OR element 6, thus increasing contents of counter 1 by "1."

The signal on input 17 will appear after the fault is set in all micro commands of all commands available in all pages of memory. This signal is the sign of completion of the fault resistance testing of the computing system.

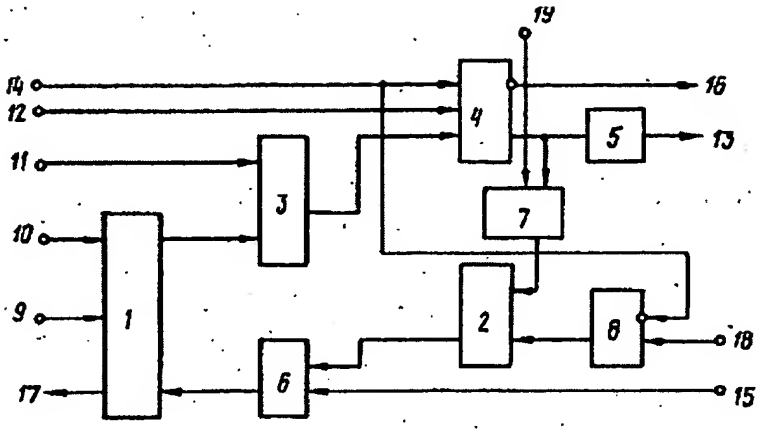
Therefore, the proposed device allows through cascading a more accurate point in the calculation process where the fault is inserted, which allows increasing the number of points in the calculation process where fault simulation can be performed, and therefore, ultimately

results in a more through and complete fault resistance testing of calculating and computing systems.

Formula of the Invention

The fault simulation device consists of two counters, the comparison block, trigger, impulse driver, two OR elements, and an AND element. The first entry point of the comparison block is also the input for the current device address; the entry point of the trigger is the input for the device identifier; the direct output of the trigger is connected with the first input of the first OR element, the output of the impulse driver is the output of the device fault simulation, which differs in the fact that with the objective of expanding its functional capacity through cascading several fault simulation devices, under any number of conditions, the information input and record input of the first counter is correspondingly the input for initial address definition and device record input. The information output of the first counter is connected with the second output of the comparison block, and the output of this block is in turn connected with the information input of trigger, the inverse output of which is at the same time the first output of the device cascading. the

direct output of the trigger is connected with the impulse driver input, the trigger reset input and inverse input of the AND element are connected with the first input of the device cascading; the second input of the first OR element is connected with the reset input of the second counter whose complementary input is connected with the output of the AND element, and whose second input also serves as the input for device time markers; the overflow output of the second counter is connected with the first input of the second OR element whose output is connected with the complementary input of the first counter, while the second input is the second output of the cascading device; the overflow output of the first counter is the second output of the device cascading.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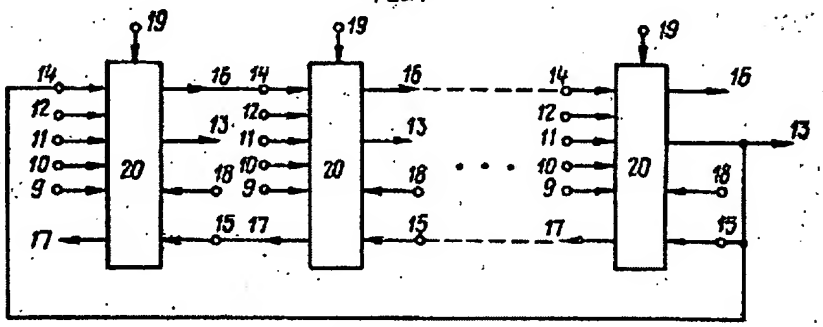
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